JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech (R13/R09) II Semester Regular/Supply Examinations July-2016

College: VASAVI,TADEPALLIGUDEM:A8

Discrepancy pertaining to these results are to be submitted on or before 30-01-2017 with following documents at CE(PG) Office,JNTUK,Kakinada

- Online Registration Proof
- Hallticket
- DForm(Online)
- DForm(Offline)
- Attendance Sheet
- Any Other supporting Documents

Htno	Subcode	Subname	Internal	External	credits
13A81D3801	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	26	-1	0
14A81D5301	H5605	SMART GRID	31	20	0
14A81D6805	H6804	DESIGN FOR TESTABILITY	30	44	1
14A81D6805	H6809	LOW POWER VLSI DESIGN	35	29	1
14A81D6809	H6804	DESIGN FOR TESTABILITY	27	36	1
14A81D6809	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	27	7	0
14A81D6811	H6804	DESIGN FOR TESTABILITY	27	42	1
15A81D1501	H1501	OPTIMIZATION AND RELIABILITY	37	37	3
15A81D1501	H1502	EXPERIMENTAL STRESS ANALYSIS	33	33	3
15A81D1501	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	34	24	3
15A81D1501	H1507	TRIBOLOGY ELECTIVE-III	28	27	3
15A81D1501	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	34	29	3
15A81D1501	H1514	DESIGN PRACTICE LAB	35	54	2
15A81D1501	H2103	FINITE ELEMENT METHOD	40	27	3
15A81D1502	H1501	OPTIMIZATION AND RELIABILITY	37	32	3
15A81D1502	H1502	EXPERIMENTAL STRESS ANALYSIS	32	36	3
15A81D1502	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	34	24	3
15A81D1502	H1507	TRIBOLOGY ELECTIVE-III	28	40	3
15A81D1502	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	36	28	3
15A81D1502	H1514	DESIGN PRACTICE LAB	37	55	2
15A81D1502	H2103	FINITE ELEMENT METHOD	38	24	3
15A81D1503	H1501	OPTIMIZATION AND RELIABILITY	37	37	3
15A81D1503	H1502	EXPERIMENTAL STRESS ANALYSIS	33	40	3
15A81D1503	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	34	28	3
15A81D1503	H1507	TRIBOLOGY ELECTIVE-III	30	32	3
15A81D1503	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	34	31	3
15A81D1503	H1514	DESIGN PRACTICE LAB	36	53	2
15A81D1503	H2103	FINITE ELEMENT METHOD	39	29	3
15A81D1504	H1501	OPTIMIZATION AND RELIABILITY	37	40	3
15A81D1504	H1502	EXPERIMENTAL STRESS ANALYSIS	34	36	3
15A81D1504	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	34	37	3
15A81D1504	H1507	TRIBOLOGY ELECTIVE-III	28	48	3
15A81D1504	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	37	32	3
15A81D1504	H1514	DESIGN PRACTICE LAB	34	56	2

Htno	Subcode	Subname	Internal	External	credits
15A81D1504	H2103	FINITE ELEMENT METHOD	40	34	3
15A81D1505	H1501	OPTIMIZATION AND RELIABILITY	37	40	3
15A81D1505	H1502	EXPERIMENTAL STRESS ANALYSIS	36	51	3
15A81D1505	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	37	32	3
15A81D1505	H1507	TRIBOLOGY ELECTIVE-III	33	43	3
15A81D1505	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	39	38	3
15A81D1505	H1514	DESIGN PRACTICE LAB	39	57	2
15A81D1505	H2103	FINITE ELEMENT METHOD	40	31	3
15A81D1506	H1501	OPTIMIZATION AND RELIABILITY	37	30	3
15A81D1506	H1502	EXPERIMENTAL STRESS ANALYSIS	31	34	3
15A81D1506	H1505	DESIGN FOR MANUFACTURING ELECTIVE-II	35	33	3
15A81D1506	H1507	TRIBOLOGY ELECTIVE-III	28	29	3
15A81D1506	H1511	MECHANICS OF COMPOSITE MATERIALS ELECTIV	37	31	3
15A81D1506	H1514	DESIGN PRACTICE LAB	38	55	2
15A81D1506	H2103	FINITE ELEMENT METHOD	40	27	3
15A81D3801	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	30	30	3
15A81D3801	H3801	CODING THEORY & APPLICATIONS	32	44	3
15A81D3801	H3803	ADVANCED COMMUNICATIONS LAB	39	58	2
15A81D3801	H4502	IMAGE & VIDEO PROCESSING	33	37	3
15A81D3801	H4503	WIRELESS COMMUNICATION & NETWORKS	32	37	3
15A81D3801	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	32	52	3
15A81D3801	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	34	24	3
15A81D3802	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	32	44	3
15A81D3802	H3801	CODING THEORY & APPLICATIONS	37	55	3
15A81D3802	H3803	ADVANCED COMMUNICATIONS LAB	39	59	2
15A81D3802	H4502	IMAGE & VIDEO PROCESSING	33	35	3
15A81D3802	H4503	WIRELESS COMMUNICATION & NETWORKS	37	38	3
15A81D3802	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	35	51	3
15A81D3802	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	37	27	3
15A81D3803	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	30	36	3
15A81D3803	H3801	CODING THEORY & APPLICATIONS	30	41	3
15A81D3803	H3803	ADVANCED COMMUNICATIONS LAB	40	57	2
15A81D3803	H4502	IMAGE & VIDEO PROCESSING	33	38	3
15A81D3803	H4503	WIRELESS COMMUNICATION & NETWORKS	31	30	3
15A81D3803	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	30	47	3
15A81D3803	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	31	24	3
15A81D3804	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	23	29	3
15A81D3804	H3801	CODING THEORY & APPLICATIONS	27	24	3
15A81D3804	H3803	ADVANCED COMMUNICATIONS LAB	39	54	2
15A81D3804	H4502	IMAGE & VIDEO PROCESSING	32	33	3
15A81D3804	H4503	WIRELESS COMMUNICATION & NETWORKS	30	29	3
15A81D3804	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	28	37	3
15A81D3804	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	31	13	0
15A81D3805	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	30	43	3
15A81D3805	H3801	CODING THEORY & APPLICATIONS	33	29	3
15A81D3805	H3803	ADVANCED COMMUNICATIONS LAB	40	58	2
15A81D3805	H4502	IMAGE & VIDEO PROCESSING	34	34	3
15A81D3805	H4503	WIRELESS COMMUNICATION & NETWORKS	36	46	3
15A81D3805	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	32	57	3
15A81D3805	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	28	3
15A81D4301	H4301	SWITCHED MODE POWER CONVERSION	38	27	3

Htno	Subcode	Subname	Internal	External	credits
15A81D4301	H4302	ELECTRIC DRIVES-II	26	39	3
15A81D4301	H4303	DIGITAL CONTROLLERS	29	28	3
15A81D4301	H4304	CUSTOM POWER DEVICES	38	26	3
15A81D4301	H4305	RENEWABLE ENERGY SYSTEMS ELECTIVE-III	31	31	3
15A81D4301	H4310	POWER CONVERTERS & DRIVES LAB	36	55	2
15A81D4301	H5605	SMART GRID	39	32	3
15A81D4302	H4301	SWITCHED MODE POWER CONVERSION	40	31	3
15A81D4302	H4302	ELECTRIC DRIVES-II	40	54	3
15A81D4302	H4303	DIGITAL CONTROLLERS	36	38	3
15A81D4302	H4304	CUSTOM POWER DEVICES	39	44	3
15A81D4302	H4305	RENEWABLE ENERGY SYSTEMS ELECTIVE-III	35	43	3
15A81D4302	H4310	POWER CONVERTERS & DRIVES LAB	39	60	2
15A81D4302	H5605	SMART GRID	40	46	3
15A81D4303	H4301	SWITCHED MODE POWER CONVERSION	40	32	3
15A81D4303	H4302	ELECTRIC DRIVES-II	39	49	3
15A81D4303	H4303	DIGITAL CONTROLLERS	37	28	3
15A81D4303	H4304	CUSTOM POWER DEVICES	39	35	3
15A81D4303	H4305	RENEWABLE ENERGY SYSTEMS ELECTIVE-III	39	36	3
15A81D4303	H4310	POWER CONVERTERS & DRIVES LAB	40	59	2
15A81D4303	H5605	SMART GRID	40	42	3
15A81D4304	H4301	SWITCHED MODE POWER CONVERSION	34	24	3
15A81D4304	H4302	ELECTRIC DRIVES-II	29	34	3
15A81D4304	H4303	DIGITAL CONTROLLERS	32	32	3
15A81D4304	H4304	CUSTOM POWER DEVICES	38	27	3
15A81D4304	H4305	RENEWABLE ENERGY SYSTEMS ELECTIVE-III	29	24	3
15A81D4304	H4310	POWER CONVERTERS & DRIVES LAB	36	52	2
15A81D4304	H5605	SMART GRID	39	11	0
15A81D5301	H5601	POWER SYSTEM DYNAMICS AND STABILITY	36	30	3
15A81D5301	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	33	8	0
15A81D5301	H5603	REAL TIME CONTROL OF POWER SYSTEMS	39	40	3
15A81D5301	H5604	ADVANCED POWER SYSTEM PROTECTION	39	40	3
15A81D5301	H5605	SMART GRID	39	24	3
15A81D5301	H5610	HIGH VOLTAGE TESTING TECHNIQUES	34	37	3
15A81D5301	H5613	POWER SYSTEMS LAB	40	53	2
15A81D5302	H5601	POWER SYSTEM DYNAMICS AND STABILITY	37	35	3
15A81D5302	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	32	30	3
15A81D5302	H5603	REAL TIME CONTROL OF POWER SYSTEMS	38	56	3
15A81D5302	H5604	ADVANCED POWER SYSTEM PROTECTION	39	28	3
15A81D5302	H5605	SMART GRID	39	24	3
15A81D5302	H5610	HIGH VOLTAGE TESTING TECHNIQUES	32	44	3
15A81D5302	H5613	POWER SYSTEMS LAB	40	52	2
15A81D5303	H5601	POWER SYSTEM DYNAMICS AND STABILITY	37	35	3
15A81D5303	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	33	34	3
15A81D5303	H5603	REAL TIME CONTROL OF POWER SYSTEMS	37	56	3
15A81D5303	H5604	ADVANCED POWER SYSTEM PROTECTION	39	31	3
15A81D5303	H5605	SMART GRID	38	34	3
15A81D5303	H5610	HIGH VOLTAGE TESTING TECHNIQUES	36	39	3
15A81D5303	H5613	POWER SYSTEMS LAB	38	50	2
15A81D5304	H5601	POWER SYSTEM DYNAMICS AND STABILITY	30	5	0
15A81D5304	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	20	16	0
15A81D5304	H5603	REAL TIME CONTROL OF POWER SYSTEMS	31	29	3

Htno	Subcode	Subname	Internal	External	credits
15A81D5304	H5604	ADVANCED POWER SYSTEM PROTECTION	30	1	0
15A81D5304	H5605	SMART GRID	35	13	0
15A81D5304	H5610	HIGH VOLTAGE TESTING TECHNIQUES	15	24	0
15A81D5304	H5613	POWER SYSTEMS LAB	35	48	2
15A81D5305	H5601	POWER SYSTEM DYNAMICS AND STABILITY	38	45	3
15A81D5305	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	31	30	3
15A81D5305	H5603	REAL TIME CONTROL OF POWER SYSTEMS	36	35	3
15A81D5305	H5604	ADVANCED POWER SYSTEM PROTECTION	39	41	3
15A81D5305	H5605	SMART GRID	39	41	3
15A81D5305	H5610	HIGH VOLTAGE TESTING TECHNIQUES	35	60	3
15A81D5305	H5613	POWER SYSTEMS LAB	37	51	2
15A81D5306	H5601	POWER SYSTEM DYNAMICS AND STABILITY	39	41	3
15A81D5306	H5602	FLEXIBLE AC TRANSMISSION SYSTEMS	35	27	3
15A81D5306	H5603	REAL TIME CONTROL OF POWER SYSTEMS	39	43	3
15A81D5306	H5604	ADVANCED POWER SYSTEM PROTECTION	39	36	3
15A81D5306	H5605	SMART GRID	39	35	3
15A81D5306	H5610	HIGH VOLTAGE TESTING TECHNIQUES	34	56	3
15A81D5306	H5613	POWER SYSTEMS LAB	40	53	2
15A81D5801	H0501	DATA WAREHOUSING AND DATA MINING	34	47	3
15A81D5801	H0507	HUMAN COMPUTER INTERACTION	38	29	3
15A81D5801	H2508	CLOUD COMPUTING	35	34	3
15A81D5801	H4002	INFORMATION SECURITY	40	41	3
15A81D5801	H5801	COMPUTER NETWORKS	36	38	3
15A81D5801	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	33	38	3
15A81D5801	H5806	CSE LAB-2	39	57	3
15A81D5802	H0501	DATA WAREHOUSING AND DATA MINING	29	12	0
15A81D5802	H0507	HUMAN COMPUTER INTERACTION	33	27	3
15A81D5802	H2508	CLOUD COMPUTING	33	26	3
15A81D5802	H4002	INFORMATION SECURITY	29	24	3
15A81D5802	H5801	COMPUTER NETWORKS	23	27	3
15A81D5802	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	18	25	0
15A81D5802	H5806	CSE LAB-2	31	47	3
15A81D5803	H0501	DATA WAREHOUSING AND DATA MINING	33	47	3
15A81D5803	H0507	HUMAN COMPUTER INTERACTION	37	29	3
15A81D5803	H2508	CLOUD COMPUTING	36	40	3
15A81D5803	H4002	INFORMATION SECURITY	39	42	3
15A81D5803	H5801	COMPUTER NETWORKS	37	45	3
15A81D5803	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	38	43	3
15A81D5803	H5806	CSE LAB-2	39	58	3
15A81D5804	H0501	DATA WAREHOUSING AND DATA MINING	34	31	3
15A81D5804	H0507	HUMAN COMPUTER INTERACTION	34	27	3
15A81D5804	H2508	CLOUD COMPUTING	34	29	3
15A81D5804	H4002	INFORMATION SECURITY	36	31	3
15A81D5804	H5801	COMPUTER NETWORKS	30	24	3
15A81D5804	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	34	26	3
15A81D5804	H5806	CSE LAB-2	38	54	3
15A81D5805	H0501	DATA WAREHOUSING AND DATA MINING	24	12	0
15A81D5805	H0507	HUMAN COMPUTER INTERACTION	33	24	3
15A81D5805	H2508	CLOUD COMPUTING	29	26	3
15A81D5805	H4002	INFORMATION SECURITY	25	8	0
15A81D5805	H5801	COMPUTER NETWORKS	21	5	0

Htno	Subcode	Subname	Internal	External	credits
15A81D5805	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	21	14	0
15A81D5805	H5806	CSE LAB-2	32	46	3
15A81D5806	H0501	DATA WAREHOUSING AND DATA MINING	30	17	0
15A81D5806	H0507	HUMAN COMPUTER INTERACTION	37	27	3
15A81D5806	H2508	CLOUD COMPUTING	35	29	3
15A81D5806	H4002	INFORMATION SECURITY	37	11	0
15A81D5806	H5801	COMPUTER NETWORKS	32	27	3
15A81D5806	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	34	34	3
15A81D5806	H5806	CSE LAB-2	38	50	3
15A81D5807	H0501	DATA WAREHOUSING AND DATA MINING	30	30	3
15A81D5807	H0507	HUMAN COMPUTER INTERACTION	37	28	3
15A81D5807	H2508	CLOUD COMPUTING	33	28	3
15A81D5807	H4002	INFORMATION SECURITY	38	24	3
15A81D5807	H5801	COMPUTER NETWORKS	31	31	3
15A81D5807	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	30	31	3
15A81D5807	H5806	CSE LAB-2	35	56	3
15A81D5808	H0501	DATA WAREHOUSING AND DATA MINING	29	28	3
15A81D5808	H0507	HUMAN COMPUTER INTERACTION	35	26	3
15A81D5808	H2508	CLOUD COMPUTING	32	24	3
15A81D5808	H4002	INFORMATION SECURITY	33	24	3
15A81D5808	H5801	COMPUTER NETWORKS	30	28	3
15A81D5808	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	29	32	3
15A81D5808	H5806	CSE LAB-2	38	59	3
15A81D5809	H0501	DATA WAREHOUSING AND DATA MINING	32	25	3
15A81D5809	H0507	HUMAN COMPUTER INTERACTION	36	27	3
15A81D5809	H2508	CLOUD COMPUTING	33	25	3
15A81D5809	H4002	INFORMATION SECURITY	38	32	3
15A81D5809	H5801	COMPUTER NETWORKS	32	27	3
15A81D5809	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	29	32	3
15A81D5809	H5806	CSE LAB-2	39	54	3
15A81D5810	H0501	DATA WAREHOUSING AND DATA MINING	33	41	3
15A81D5810	H0507	HUMAN COMPUTER INTERACTION	33	24	3
15A81D5810	H2508	CLOUD COMPUTING	35	36	3
15A81D5810	H4002	INFORMATION SECURITY	38	45	3
15A81D5810	H5801	COMPUTER NETWORKS	35	33	3
15A81D5810	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	31	37	3
15A81D5810	H5806	CSE LAB-2	39	59	3
15A81D5811	H0501	DATA WAREHOUSING AND DATA MINING	32	34	3
15A81D5811	H0507	HUMAN COMPUTER INTERACTION	36	28	3
15A81D5811	H2508	CLOUD COMPUTING	32	26	3
15A81D5811	H4002	INFORMATION SECURITY	38	33	3
15A81D5811	H5801	COMPUTER NETWORKS	32	27	3
15A81D5811	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	29	28	3
15A81D5811	H5806	CSE LAB-2	36	54	3
15A81D6801	H6801	EMBEDDED-C	31	27	3
15A81D6801	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	26	28	3
15A81D6801	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	28	51	3
15A81D6801	H6804	DESIGN FOR TESTABILITY	34	46	3
15A81D6801	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	33	33	3
15A81D6801	H6809	LOW POWER VLSI DESIGN	26	34	3
15A81D6801	H6811	EMBEDDED SYSTEMS LAB	33	50	2

Htno	Subcode	Subname	Internal	External	credits
15A81D6802	H6801	EMBEDDED-C	33	24	3
15A81D6802	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	36	25	3
15A81D6802	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	28	40	3
15A81D6802	H6804	DESIGN FOR TESTABILITY	36	39	3
15A81D6802	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	24	3
15A81D6802	H6809	LOW POWER VLSI DESIGN	32	25	3
15A81D6802	H6811	EMBEDDED SYSTEMS LAB	37	57	2
15A81D6803	H6801	EMBEDDED-C	33	29	3
15A81D6803	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	28	28	3
15A81D6803	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	33	47	3
15A81D6803	H6804	DESIGN FOR TESTABILITY	37	40	3
15A81D6803	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	32	30	3
15A81D6803	H6809	LOW POWER VLSI DESIGN	33	37	3
15A81D6803	H6811	EMBEDDED SYSTEMS LAB	36	57	2
15A81D6804	H6801	EMBEDDED-C	32	24	3
15A81D6804	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	26	28	3
15A81D6804	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	30	40	3
15A81D6804	H6804	DESIGN FOR TESTABILITY	35	37	3
15A81D6804	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	34	30	3
15A81D6804	H6809	LOW POWER VLSI DESIGN	29	35	3
15A81D6804	H6811	EMBEDDED SYSTEMS LAB	37	54	2
15A81D6805	H6801	EMBEDDED-C	26	8	0
15A81D6805	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	28	24	3
15A81D6805	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	27	24	3
15A81D6805	H6804	DESIGN FOR TESTABILITY	28	31	3
15A81D6805	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	26	1	0
15A81D6805	H6809	LOW POWER VLSI DESIGN	21	29	3
15A81D6805	H6811	EMBEDDED SYSTEMS LAB	35	56	2
15A81D6806	H6801	EMBEDDED-C	34	24	3
15A81D6806	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	32	33	3
15A81D6806	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	31	51	3
15A81D6806	H6804	DESIGN FOR TESTABILITY	37	48	3
15A81D6806	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	31	3
15A81D6806	H6809	LOW POWER VLSI DESIGN	37	32	3
15A81D6806	H6811	EMBEDDED SYSTEMS LAB	34	57	2
15A81D8701	H8701	FINITE ELEMENT METHOD	32	46	3
15A81D8701	H8702	EARTHQUAKE RESISTANT DESIGN	33	32	3
15A81D8701	H8703	STABILITY OF STRUCTURES	31	24	3
15A81D8701	H8704	THEORY OF PLATES & SHELLS	34	30	3
15A81D8701	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	19	31	3
15A81D8701	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	26	33	3
15A81D8701	H8711	CAD LAB	32	52	2
15A81D8702	H8701	FINITE ELEMENT METHOD	31	45	3
15A81D8702	H8702	EARTHQUAKE RESISTANT DESIGN	33	34	3
15A81D8702	H8703	STABILITY OF STRUCTURES	36	35	3
15A81D8702	H8704	THEORY OF PLATES & SHELLS	37	34	3
15A81D8702	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	32	26	3
15A81D8702	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	34	31	3
15A81D8702	H8711	CAD LAB	33	52	2
15A81D8703	H8701	FINITE ELEMENT METHOD	28	41	3
15A81D8703	H8702	EARTHQUAKE RESISTANT DESIGN	31	30	3

Htno	Subcode	Subname	Internal	External	credits
15A81D8703	H8703	STABILITY OF STRUCTURES	35	30	3
15A81D8703	H8704	THEORY OF PLATES & SHELLS	37	28	3
15A81D8703	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	26	33	3
15A81D8703	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	32	27	3
15A81D8703	H8711	CAD LAB	35	52	2
15A81D8704	H8701	FINITE ELEMENT METHOD	31	35	3
15A81D8704	H8702	EARTHQUAKE RESISTANT DESIGN	33	24	3
15A81D8704	H8703	STABILITY OF STRUCTURES	32	24	3
15A81D8704	H8704	THEORY OF PLATES & SHELLS	38	32	3
15A81D8704	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	28	26	3
15A81D8704	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	26	18	0
15A81D8704	H8711	CAD LAB	28	42	2
15A81D8705	H8701	FINITE ELEMENT METHOD	26	30	3
15A81D8705	H8702	EARTHQUAKE RESISTANT DESIGN	26	24	3
15A81D8705	H8703	STABILITY OF STRUCTURES	27	29	3
15A81D8705	H8704	THEORY OF PLATES & SHELLS	36	35	3
15A81D8705	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	24	26	3
15A81D8705	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	27	24	3
15A81D8705	H8711	CAD LAB	30	44	2
15A81D8706	H8701	FINITE ELEMENT METHOD	38	50	3
15A81D8706	H8702	EARTHQUAKE RESISTANT DESIGN	39	37	3
15A81D8706	H8703	STABILITY OF STRUCTURES	38	39	3
15A81D8706	H8704	THEORY OF PLATES & SHELLS	40	52	3
15A81D8706	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	35	40	3
15A81D8706	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	34	34	3
15A81D8706	H8711	CAD LAB	38	55	2
15A81D8707	H8701	FINITE ELEMENT METHOD	29	45	3
15A81D8707	H8702	EARTHQUAKE RESISTANT DESIGN	28	29	3
15A81D8707	H8703	STABILITY OF STRUCTURES	28	24	3
15A81D8707	H8704	THEORY OF PLATES & SHELLS	31	28	3
15A81D8707	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	23	27	3
15A81D8707	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	21	24	0
15A81D8707	H8711	CAD LAB	31	43	2

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **03-02-2017]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:4
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

Date:21-01-2017

Controller of Examinations