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SRI VASAVI ENGINEERING COLLEGE

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Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

Department of Electronics and Communication Engineering

Academic Year: 2017-18

Programme : ECE	Class/Sem: IV B. Tech(I-Sem)	Sec: A, B & C
Course Code: RT42041		Course Title: VLSI DESIGN

UNIT WISE QUESTION BANK

UNIT-1

1. List the steps involved in IC fabrication.[CO1:K1]
2. Explain about various IC technologies . [CO1:K2]
3. Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode. [CO1:K2]
4. Explain the MOS transistor operation with the help of neat sketches in the Depletion mode. [CO1:K2]
5. Find the expression for the threshold voltage of MOSFET. [CO2:K2]
6. Explain the term output conductance, using necessary equations. [CO2:K2]
7. Explain the figure of merit of a MOS transistor. [CO2:K2]
8. Explain how the BiCMOS inverter performance can be improved. [CO2:K2]
9. Explain the operation of an nMOS inverter with a neat diagram. [CO2:K2]
10. Explain the nMOS enhancement mode fabrication process for different conditions of Vds? [CO2:K2]
11. Write down the equations for Ids of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region? [CO2:K1]
12. Find an equation for transconductance of an n-channel enhancement MOSFET operating in active region. [CO2:K1]

UNIT-2

1. Define stick diagram and layout diagram? [CO3:K1]
2. Design a stick diagram for NMOS EX-OR gate. [CO3:K3]
3. Draw the circuit diagram for CMOS two-input NAND gates. [CO3:K3]
4. What are scalable design rules and list its disadvantages. [CO3:K1]
5. Draw the mask layout of 1-bit CMOS shift register cell. [CO3:K3]
6. Define Fan-in and Fan-out. [CO3:K1]
7. Explain about pass transistor and pass transistor gates. [CO3:K2]
8. Explain MOS layers with a neat sketch. [CO3:K2]
9. Explain 2µm CMOS design rule for wires? [CO3:K2]
10. Draw the stick diagram and mask layout for CMOS two input NOR gate and stick diagram of two input NAND gates. [CO3:K3]
11. What are the different types of design rules? Explain. [CO3:K2]
12. What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter[CO3:K3]
13. Explain 2µm Double Metal, Double Poly. CMOS / BiCMOS Rules. [CO3:K2]

UNIT-3

1. List out the limitations of scaling? [CO4:K1]
2. Define inverter delay? Explain. [CO4:K1]
3. Define scaling factor? Explain different types of device parameters. [CO4:K2]
4. What are the sources of wiring capacitances? [CO4:K1]
5. Discuss about nMOS transistor as a switch and pMOS transistor as a switch. [CO4:K2]
6. Define standard unit capacitance? Explain. [CO4:K2]

7. What are the limits on logic levels and supply voltage due to noise in scaling? [CO4:K1]
8. Realize the NAND gate using nMOS technology. [CO4:K3]
9. What are the issues involved in driving large capacitor loads in VLSI circuit regions? Explain. [CO4:K2]
10. Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel value is 4x10-4 pF/mm2 . [CO4:K3]

UNIT-4

1. Explain bus arbitration logic for n-line bus structured design approach. [CO5:K2]
2. Explain two-phase clocking. [CO5:K2]
3. Explain the structured design approach of parity generator. [CO5:K2]
4. What is pre-charged bus concept? [CO5:K1]
5. Discuss some system considerations. [CO5:K2]
6. What are the advantages and disadvantages of dynamic logic? [CO5:K1]
7. Write about dynamic register element. [CO5:K2]
8. Explain the design of a 4-bit shifter. [CO5:K2]
9. Discuss the general arrangement of a 4-bit arithmetic process. [CO5:K2]
10. Explain the basic structure of a dynamic CMOS gate? [CO5:K2]
11. How switch logic can be implemented using Pass Transistors? Explain. [CO5:K2]
12. Draw the transistor circuit diagram of shift register capable of holding and shifting 4-bit word. Explain the circuit operation. [CO5:K2]
13. Explain charge storage. [CO5:K2]

UNIT-5

1. Explain the single Stuck-at Fault model. [CO6:K2]
2. Discuss the ASIC design flow. [CO6:K2]
3. Give the overflow of system on chip designs. [CO6:K1]
4. Explain the FPGA design flow. [CO6:K2]
5. Give the advantages and disadvantages of cell based design. [CO6:K1]
6. Write the steps to resolve the clock skew problem. [CO6:K2]
7. Explain switch logic? [CO6:K2]
8. Discuss the design process for developing a chip. [CO6:K2]
9. Compare Full-Custom design with semi-custom design. [CO6:K2]
10. Explain mixed signal design with neat sketch. [CO6:K2]
11. Discuss the clock mechanisms. [CO6:K2]
12. List out the back-end steps in ASIC design flow? [CO6:K1]
13. List out the front-end steps in FPGA design flow? [CO6:K1]
14. What are FPGAs? Explain the principle and operation. [CO6:K2]
15. Write note on package solution. [CO6:K2]
16. Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming. [CO6:K2]
17. What is testing? Explain. [CO6:K2]

UNIT-6

1. What is the need of a FPGA? And write its applications. [CO7:K2]
2. Write the steps to design an FPGA. [CO7:K2]
3. How to design FPGA-Based PCBs? Explain. [CO7:K2]
4. Write about FPGA families of different vendors. [CO7:K2]
5. Explain stack implementation using VHDL. [CO7:K2]

6. Write about configuration modes. [CO7:K2]
7. What parameters to be consider while identifying the FPGA? [CO7:K1]
8. Explain implementation of queue using VHDL. [CO7:K2]
9. Explain the basic architecture of FPGA. [CO7:K2]
10. Explain the FPGA design process. [CO7:K2]
11. Clearly explain each step of high level design flow of an ASIC. [CO7:K2]
12. Write a short note on mixed signal design? [CO7:K2]