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SRI VASAVI ENGINEERING COLLEGE

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

Department of Electronics and Communication Engineering

Low Power IC Design

UNIT-WISE QUESTION BANK

UNIT-1

1. Write the need for Low Power VLSI.
2. List out the sources of power dissipation in VLSI circuits and explain any two in detail.
3. Write about sources of leakage power with neat diagram.
4. Write about Drain Induced Barrier Lowering of NMOS transistor.
5. Explain about switching power dissipation and short circuit power dissipation.
6. Explain about Glitching power dissipation
7. Briefly explain about velocity saturation.
8. Briefly explain about short channel effects of a transistor.

UNIT-2

1. Write the advantages of Voltage scaling.
2. With a neat sketch, explain a variable threshold CMOS inverter circuit.
3. With a neat sketch, explain a multiple threshold CMOS inverter circuit.
4. Write about pipelining and parallel processing.
5. Write the advantages and disadvantages of MTCMOS circuits.
6. Compare pipelining and parallel processing approaches.

UNIT-3

1. Explain the computing resources and its accuracy at various levels of abstraction.
2. Write about SPICE circuit simulator.
3. Explain about Gate-level logic simulation.
4. Explain the capacitive power dissipation of the circuit.
5. Explain the power analysis at various levels of abstraction.
6. Estimate various sources of capacitance for gate level power analysis.

UNIT-4

1. Realize CMOS logic for 1 bit full adder.
2. Write the drawbacks of ripple carry adder.
3. Write the drawbacks of carry look ahead adder.
4. Design a carry-out circuit of 4 bit carry look ahead adder

5. Write down the differences between carry select adders and carry save adders.
6. Discuss any two types of low voltage low power logic styles.
7. Draw the logic circuit of the conventional CMOS full adder and explain about it.
8. Explain the basic theory, operation and performance evaluation of carry look-ahead adders.
9. Explain the basic theory, operation and performance evaluation of MCC adder.

UNIT-5

1. What are the building blocks are needed for binary array multiplier and explain
2. Construct Braun Multiplier and explain its operation
3. Draw the basic building blocks of the Baugh-Wooley multiplier architecture and explain its operation.
4. Write down the algorithm of Baugh-Wooley multiplier.
5. Discuss the types of multiplier architectures.
6. Explain about Booth multiplier.
7. Explain about Wallace tree multiplier.

UNIT-6

1. Design a 8X3 ROM and explain its operation.
2. Compare SRAM and DRAM memories.
3. Explain the necessity of two-dimensional decoding mechanism in memories.
4. Draw MOS transistor memory cell in ROM and explain the operation.
5. Compare SRAM and DRAM.
6. Give a note on future trend and development of ROM.
7. Write down differences between 6T and 4T static RAM cells.
8. With a neat diagram, explain the block diagram of DRAM architecture.
9. Discuss low power SRAM technologies with neat diagrams.