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SRI VASAVI ENGINEERING COLLEGE

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

Department of Electronics and Communication Engineering

Year & SEM : III B.Tech & 1sem

Name of the Course: DSD &Digital IC Applications **Course Code: RT31044**

Unit Wise Question Bank

UNIT-1

1. Discuss the binding? Discuss the binding between entity and Architecture, Entity and Components.
2. Differentiate between Functions and Procedures in VHDL.
3. What are different data types available in VHDL? Explain.
4. Give the syntax and structure of a Package in VHDL with an example.
5. Write a VHDL Function to convert VECTOR to INTEGER.
6. Explain the steps in HDL-based design flow.
7. Explain about data objects in VHDL.
8. Explain about dataflow design elements of VHDL.
9. Explain about structural design elements of VHDL.
10. Explain about behavioral design elements of VHDL.
11. Write a test bench for two input XOR gate using VHDL.
12. Differentiate between VHDL and Verilog HDL.

UNIT-2

1. Define Simulation? Explain about simulations at various levels.
2. Explain about various types of Simulation.
3. What is Logic Synthesis? Explain about different processes used inside logic Synthesizer.
4. Discuss some of the important factors related to synthesis.
5. Explain about inertial and transport delay models in VHDL with examples.
6. What are the goals and objectives of global routing and detailed routing.
7. Explain about constraints used in the synthesis process and performance driven synthesis.
8. Explain about functional gate level simulation and technology libraries.
9. What are the major Netlist formats used for design representation?
10. Explain about critical reports generated during the synthesis process.
11. Discuss about place and route and post layout simulation in design process.
12. Explain about static timing analyzer.

UNIT-3

1. Design an Excess-3 to BCD code converter using PLA.
2. Design a BCD to Excess-3 code converter using PLA.
3. Implement the following Boolean function using PLA.
4. $F1(a,b,c) = \sum m(0,1,3,5)$, $F2(a,b,c) = \sum m(3,5,7)$

5. Design a BCD to GRAY code converter using PLA.
6. What are the differences between PROM, PLA and PAL.
7. What are the advantages of PLDs.
8. Explain the concept of 2D Decoding.
9. Draw and explain Bipolar and MOSFET SRAM cells.
10. Distinguish between SRAM and ROM.
11. Draw and explain internal structure of ROM using 4 byte Diode ROM.
12. List out the applications, advantages and disadvantages of ROM.
13. Determine the ROM size needed to realize the logic function performed by
14. 74x153(Dual 4 to 1 MUX) and 74x139 (Dual 2 to 4 Decoder).
15. Draw and explain timing diagram of SRAM (read and write operation)
16. Explain the internal structure of DRAM and also draw the timing diagram for read and write operations.
17. Draw the block diagram of synchronous RAM and Explain its operation with timing diagram for read and write operations.

UNIT-4

1. Design a CMOS transistor circuit for 3 input AND gate with the help of function table Explain the circuit.
2. Explain the circuit behavior with the help of resistive loads. With the help of resistive loads model explain CMOS inverter.
3. Design CMOS OR-AND-INVERT gates (OAI) with help of functional table.
4. Design Basic CMOS inverter circuit with functional table
5. Design a CMOS AND OR–INVERT gates (AOI) with help of functional table.
6. Explain the following with diagrams
   (i)CMOS Driving TTL in HIGH State (ii) CMOS Driving TTL in LOW State.
7. Draw the circuit diagram of basic TTL NAND Gate and explain the 3 pats with help of functional operation?
8. Explain about the steady state electrical behavior for
   a) Resistive Loads b) Non Ideal Inputs c) Unused Inputs d) fan-in and fan-out
9. Explain about the dynamic state electrical behavior for
   a) Power Consumption b) Transition time c) Propagation delay
10. Explain the following CMOS logic families
    (i) 4000 series CMOS(ii)HC and HCT families (iii)VHC and VHCT families
11. Design 2 input CMOS XOR and XNOR gate with help of functional table
12. What is interfacing? Explain interfacing between Low Voltage TTL and Low Voltage CMOS Logic?

13. List out the Characteristics of ECL? Design a Transistor circuit of 2-input ECL NOR gate, explain the operation with the help of function table?
14. What are the advantages and disadvantages of CMOS Technology?
15. Give the logic levels and Noise Margins of CMOS and TTL Families?
16. Compare FET and BJT?
17. Discuss about ESD, Latch-Up.

UNIT-5

18. Write a VHDL program for
    a. 4x1 Multiplexer and 1x4 Demultiplexer.
    b. Fixed point to Floating point conversion
    c. 4x2 Encoder and 2x4 decoder
    d. Full Adder using two Half Adders
    e. 4-bit look ahead carry generator
19. Design 5*32 Decoder using one 2*4 decoder and four 3*8 decoders ICs and explain its operation.
20. Implement 32 to 5 output priority encoder using four 74LS148 and gates?
21. Design a priority encoder for 16 inputs using 74x148 encoders?
22. Implement the following multiple output functions using 74LS138 and external gates.
    $F1=\Sigma m\ (1, 4, 5, 7)$, $F2=\Pi M\ (2, 3, 6, 7)$
23. Design 74x157 Quad 2i/p multiplexer and 74x153 4*1 mux with the help of logic diagram and truth tables.
24. Design 32*1 mux using two 74LS150.
25. Design logic diagram and pin diagrams of tri-state buffer ICs (74*125, 74*126, 74*541, 74*245)
26. Draw the logic diagram of IC74180 priority generator checker and explain its operation?
27. Implement the following Boolean functions using 4:1 MUX $F(A,B,C,D) =\Sigma m\ (0,1,2,4,6,9,12,14)$
28. Draw pin diagram and logic diagrams of IC 74*85,IC74*682(Comparators) and design a 16-bit comparator using IC74x85
29. Draw the interfacing diagram of ten key keypad. Interface to a digital system using Decimal to BCD Decoder (74LS147).
30. Design a 4x4 combinational multiplier and write VHDL code in dataflow style.

UNIT-6

1. Draw and explain the pin diagrams of 74*95 and 74*195.
2. Draw and explain pin diagrams and logic diagrams of IC74*175, IC 74*174, IC 74*374, IC 74373, 74*273(MSI Registers).
3. Design SSI latches and flip-flops (IC 74*74,74*112,74*109) and explain operation of D,T,JK FFs
4. Convert the following
   a. T to D flip-flop b. JK to SR flip-flop c. JK to D flip-flop
5. Design MSI Shift register ICs and logic diagrams

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6. Explain modes of shift registers(SISO,SIPO,PISO,PIPO)
7. Design a 8-bit PISO Shift Register and explain the operation with the help of timing diagrams?
8. Design a mod-100 counter using two 74x163 binary counters?
9. Design a ring counter, Johnson counter using 74x194?
10. Design an excess 3 decimal counter using 74x163 binary counter and explain the operation with the help of timing diagrams?
11. Discuss the logic circuit of 74x377 register and write VHDL program for the same in structural style?
12. Give a VHDL code for 4 bit UP counter with enable and clear inputs.
13. Design a 3 bit LFSR counter using 74194. List out the sequence assuming that the initial state is "111".
14. Draw the logic diagram of Universal shift register and explain its operation?
15. Explain how a JK flip-flop can be constructed using a T flip-flop